

# **[STRUCTURE OF FLASH MEMORY DEVICE AND FABRICATION METHOD THEREOF]**

## **Abstract of Disclosure**

A flash memory device includes a substrate having a trench, a deep N-type well region in the substrate, a stacked gate structure on the substrate, a first and a second spacer on a sidewall of the stacked gate, wherein the first spacer is connected with the top of the trench, a source region in the substrate under the first spacer, a drain region in the substrate under the second spacer, a P-type well region between the stacked gate and the deep N-type well region, wherein the junction between the two well regions is higher than the bottom of the trench, a doped region along the bottom and the sidewall of the trench, wherein this doped region is connected with the source region and isolates the P-type well region from the contact formed in the trench, the contact being electrically connected to the source region.

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